REMARKS

The Office Action dated December 13, 2004 has been received and carefully considered. In this response, claims 1 and 11 have been amended to recite the additional limitations recited by dependent claims 10 and 20, respectively. Additionally, claims 10 and 20 have been canceled and claims 23-26 have been added. Support for the amendments to claims 1 and 11 and the addition of the new claims may be found in the specification and figures as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks and in view of the merger of claims 1 and 10 and the merger of claims 11 and 20.

Anticipation Rejection of Claims 1-9 and 11-19

At page 2 of the Office Action, claims 1-9 and 11-19 were rejected under 35 U.S.C. Section 102(b) as being anticipated by Matsumura (U.S. Patent No. 5,365,475). These claims have been amended, thereby obviating this rejection.

Claim 1, from which claims 2-9 depend, has been amended to recite the additional limitations originally recited by dependent claim 10 (now canceled). Claim 11, from which claims 12-19 depend, has been similarly amended to recite the additional limitations originally recited by dependent claim 20 (now canceled). As admitted by the Examiner at pages 5-6 of the Office Action, Matsumura fails to disclose at least these limitations. Matsumura therefore fails to disclose each and every limitation of amended claims 1 and 11.

Accordingly, it is respectfully submitted that the anticipation rejection of claims 1-9 and 11-19 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Obvious Rejection of Claims 10 and 20

At page 5 of the Office Action, claims 10 and 20 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Matsumura in view of Shimazu (U.S. Patent No. 4,777,623). This rejection is respectfully traversed.

As noted above, claims 1 and 11 have been amended to recite the additional limitations originally recited by claims 10 and 20, respectively, and claims 10 and 20 have been canceled. Accordingly, claims 1 and 11 presently recite the limitations of a biasing circuit comprising a

grounding circuit selectively connected by a programmable connect to one of a first inverter output and a second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing a second I/O line to a known logic state. The Examiner admits that Matsumura fails to teach these limitations. *Office Action*, pp. 5 and 6. The Examiner therefore turns to Shimazu and asserts that the passage of Shimazu at col. 3, line 65 to col. 4, line 14 discloses these limitations. For ease of reference, this relied-upon passage of Shimazu is provided below:

> As described above, in the embodiment of FIG. 3, the ratio latch 4 can be set by merely raising the output voltage of the power source 12 which is driving the memory circuit 14 higher than the output voltage at the ordinary operation. Accordingly, there is neither the necessity of wiring the set signal input line for transmitting a set initialization signal, nor the necessity of the set initialization signal input terminal, thereby enabling the implementation of a larger scale integration.
>
> Meanwhile, the switching of the output voltage of the power source 12 is readily performed by forming a power supply circuit (not shown) provided in the outside of the memory circuit 14 in such a way that it could output two different voltages.
>
> As for the MOS transistor 15, such a device as having sufficient driving capability to pull down the level of the input data line to "0" even when the input data is "1" may be used.

Shimazu, col. 3, line 65-col. 4, line 14.

The Applicants respectfully submit that the relied-upon passage of Shimazu fails to disclose or suggest a grounding circuit *selectively* connected *by a programmable select* to one of a first inverter output or a second inverter output as originally recited by claims 10 and 20 and presently recited by amended claims 1 and 11. Instead, Figure 3 of Shimazu and the above relied-upon passage of Shimazu merely disclose a transistor 15*fixedly* coupled to the output of the inverter 3 at one node and to ground at another. Shimazu fails to disclose or suggest that the transistor 15 (which the Examiner appears to consider equivalent to the grounding circuit limitation of claims 1 and 11) is *selectively* connected to one of the outputs of the inverters 2 and 3 as recited by claims 1 and 11. Moreover, Shimazu provides no disclosure or suggestion that the transistor 15 is connected to the output of the inverter 3 by a*programmable connect*, so Shimazu necessarily fails to disclose or suggest a grounding circuit *selectively* connected by a *programmable co nnec*t as recited by claims 1 and 11.

It is further submitted that the relied-upon passage of Shimazu fails to provide any disclosure related to temporarily enabling the transistor 15 upon powering on the memory cell. Accordingly, Shimazu also fails to disclose or suggest the limitations of wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device as recited by claims 1 and 11.

Moreover, the Applicants respectfully submit that there is no motivation to combine the teachings of Matsumura and Shimazu as proposed by the Examiner. Matsumura teaches a technique whereby the inputs and outputs of two inverters of a memory cell are connected in various ways to two ground lines (G1, G2) and two supply lines (V1, V2) so as to configure the memory cell to be a ROM cell storing a value of 1, a ROM cell storing a value of 0 or a RAM cell depending on the particular connection to the lines and the voltages applied to the lines. *See, e.g., Matsumura*, Figures 3-8A. In contrast, Shimazu teaches a technique whereby signal lines (e.g., set signal 7a of "prior-art" Figure 1 or reset signal 13a of "prior-art" Figure 2) may be omitted by varying the voltage of a power supply that powers the entire memory cell so as to cause a transistor to source the input of an inverter to logic high or low depending on the particular configuration. Thus, while Matsumura teaches using supply lines so as to configure a memory cell to function in a certain manner, Shimazu teaches the avoidance of such supply lines. Thus, the Examiner's proposed combination of Matsumura and Shimazu finds no motivation in the teachings of either of Matsumura and Shimazu as the Examiner relies on the irreconcilable teachings of the use of such supply lines as taught by Matsumura and the elimination of such lines as taught by Shimazu.

As there is no motivation to combine the teachings of Matsumura and Shimazu as proposed by the Examiner and as Matsumura and Shimazu fail to disclose each and every limitation of amended claims 1 and 11 even if combined as proposed, it is respectfully submitted that the Office Action fails to establish a *prima facie* obvious rejection of claims 1 and 11. The Office Action therefore also fails to establish a prima facie obviousness rejection of claims 2-9 and 12-19 at least by virtue of these claims dependency from one of claims 1 or 11. Furthermore, these dependent claims recite additional limitations neither disclosed nor suggested by the cited references.

Accordingly, it is respectfully submitted that the obviousness rejection of claims 10 and 20 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Addition of New Claims 23-26

New claims 23-26 have been added. Support for the addition of these claims may be found, *inter alia*, in Figure 2 of the present application. Claims 23 and 25, which depend from claims 1 and 11, respectively, recite the additional limitations of wherein said grounding circuit comprises a first transistor comprising a first node coupled to a voltage reference, a second node selectively connected by the programmable connect to one of said first inverter output and said second inverter output and a gate node operable to receive a signal to temporarily enable the grounding circuit after power is applied to said SRAM device. Claims 24 and 26, which depend from claims 23 and 25, respectively, recite the further limitations of wherein said grounding circuit further comprises a second transistor comprising a first node coupled to the voltage reference, a second node selectively connected by a second programmable connect to one of said first inverter output and said second inverter output and a gate node operable to receive the signal to temporarily enable the grounding circuit after power is applied to said SRAM, wherein said second node of said first transistor and said second node of said second transistor are selectively coupled to different outputs of said first inverter output and said second inverter output and wherein said second transistor is an opposite bias type as said first transistor. The Applicants respectfully submit that neither Matsumura nor Shimazu disclose or suggest a first transistor connected as recited by claims 23 and 25 or a second transistor connected as recited by claims 24 and 26.

Conclusion

It is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application. The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 01-0365.

Respectfully submitted,

8 February 2005
Date

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